CBCS Scheme

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15CS34

Third Semester B.E. Degree Examination, Dec.2017/Jan.2018
Computer Organization

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. List the steps needed to execute the machine instruction Add LOCA, RO in terms of transfers between the processor and the memory along with some simple control commends. Assume that the instruction itself is stored in the memory at location INSTR and that this address is initially in register PC. The first two steps might be expressed as:
- Transfer the contents of Register PC to register MAR.
- Issue a Read command to the memory and then wait until it has transferred the requested word into register MDR.

Remember to include the steps needed to update the contents of PC from INSTR to INSTR+1 so that the next instruction can be fetched. **(08 Marks)**

b. What is performance measurement? Explain the overall SPEC rating for the computer in a program suit. **(08 Marks)**

OR

2 a. With relevant figure define the little Endian and big Endian assignments. **(04 Marks)**

b. Consider a computer that has a byte addressable memory organized in 32 bit words according to the big Endian scheme. A program reads ASCII characters entered at a keyboard and store them in successive byte location starting at location 1000. Show the contents of the two memory words at locations 1000 and 1004 after the name "Johnson" has been entered. (ASCII codes J = 4 AH, o = 6 FH, h = 68 H, n = 6 EH, S = 73 H) **(04 Marks)**

c. Write about shift and rotate instruction with neat diagram and example of each. **(08 Marks)**

Module-2

3 a. With supporting diagram, explain the following with respect to interrupts:
i) Vectored interrupts
ii) Interrupt Nesting
iii) Simultaneous requests. **(06 Marks)**

b. Three devices A, B and C are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed, but interrupt requests from C may be accepted while either A or B is being services. Suggest different ways in which this can be accomplished in each of the following cases:
i) The computer has one interrupt request line.
ii) Two interrupt request line, INTR1 and INTR2 are available with INTR1 having higher priority. Specify when and how interrupts are enabled and disable in each case. **(06 Marks)**

c. Illustrate the tree structure of USB with diagram. **(04 Marks)**

OR

4 a. With a neat diagram, explain the centralized arbitration and distributed bus arbitration scheme. **(08 Marks)**

b. With neat timing diagram illustrate the asynchronous bus data transfer during an input operation. Use handshake scheme. **(08 Marks)**

Module-3

5 a. Draw a diagram and explain the working of 16 Megabit DRAM chip configured as 2M × 8. **(08 Marks)**

b. Describe organization of an 2M × 32 memory using 512K × 8 memory chips. **(08 Marks)**

OR

6 a. Discuss in detail the working of set associative mapped cache with two blocks per set with relevant diagram. **(08 Marks)**

b. Define the following with respect to cache memory: (i) Valid bit, (ii) Dirty data, (iii) Stale data, (iv) Flush the cache. **(04 Marks)**

c. A block-set associative cache consists of a total of 64 blocks divided into 4-blocks sets. The main memory contains 4096 blocks, each consisting of 128 words.
   i) How many bits are there in a main memory address?
   ii) How many bits are there in each of the TAG, SET and WORD fields? **(04 Marks)**

Module-4

7 a. Convert the following pairs of decimal numbers to 5-bit signed 2's complement binary numbers and add them. State whether or not overflow occurs in each case.
   i) 5 and 10 ii) −14 and 11 iii) −5 and 7 iv) −10 and −13 **(04 Marks)**

b. Design the 16 bit carry look ahead adder using 4-bit adder. Also unite the expression for C_{i+1}. **(08 Marks)**

c. Draw the two n-bit number x and y to perform addition/subtraction. **(04 Marks)**

OR

8 a. With an example explain the Booths algorithm to multiply two signed operands. **(08 Marks)**

b. Multiply each of the following pairs of signed 2's complement number using the Booth algorithm. (A = multiplicand and B = multiplier).
   i) A = 010111 and B = 110110
   ii) A = 110011 and B = 101100
   iii) A = 110101 and B = 011011
   iv) A = 001111 and B = 001111 **(08 Marks)**

Module-5

9 a. Discuss with neat diagram, the single bus organization of the data path inside a processor. **(08 Marks)**

b. Write the sequence of control steps required for single bus structure for each if the following instructions.
   i) Add the contents of memory location NUM to register R1.
   ii) Add the contents of memory location whose address is at memory location NUM to register R1. **(08 Marks)**

OR

10 a. Discuss the microwave oven with neat block diagram. **(08 Marks)**

b. Discuss the digital camera with neat block diagram. **(08 Marks)**

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